UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,138	12/03/2003	Kaushik Saha	852463.406	5322

38106 7590 08/24/2010

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 5400
SEATTLE, WA 98104-7092

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
08/24/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,138	SAHA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2010 and 23 June 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7, 11-13, 15-18, 27-29 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-13,15-18,27-29 and 31-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2010* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/21/10 and 06/23/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 06/23/2010 and 06/21/2010.

2. Claims 1-7, 11-13, 15-18, 27-29 and 31-33 are pending in this application. Claims 1, 3, 5, 16, 27 and 31 are independent claims. This Office Action is made final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations within all independent claims must be shown or the feature(s) canceled from the claim(s), particularly the structure of computing/performing N-point FFT/IFFT of the signal using first and second stages wherein the second stage employs single un-nested computation loop. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-7, 11-13, 15-18, 27-29 and 31-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 1, the newly added limitations "first and second sets of butterfly computations stages… wherein the second stage employs single un-nested computation loop" have never fully addressed in the summary or detail of the invention of the original specification in a way that would be able to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention within the context of the claims. Claims 3, 5, 16, 27 and 31 have similar rejection.

Thus, claims 2, 4, 6-7, 11-13, 15, 17-18, 28-29 and 32-33 are also rejected for being dependent on the rejected base claims 1, 3, 5, 16, 27 and 31 respectively.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 7, 11-13, 15, 27-29 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abel et al. (U.S. 5,991,787) in view of Jaber (U.S. 6,792,441).

Re claim 1, Abel et al. disclose in Figures 1-14 method of processing a digital signal by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) of the digital signal (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT), the method comprising the steps of: computing an N-point FFT/IFFT of a signal (e.g. either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively) using first and second sets of butterfly computational stages (e.g. Figure 4 and Figure 8 wherein the first plurality of butterfly is performed in components 800 and 805), each stage in the second set of stages employing a plurality of butterfly operations (e.g. Figure 8 wherein components 800 and 805 each utilizes radix-2 as the first radix size) wherein each of the butterfly operations in each stage (e.g. components 800, 805, and 810 in Figure 8) in the second set of stages has a single, un-nested computation loop (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT).

Abel et al. fail to disclose in Figures 1-14 a method comprising using a multiprocessing computing system having a plurality of processors P to perform the steps

and for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency among the parallel processors. However, Jaber discloses in Figures 8-9 a method (e.g. by means of independent and distribute among processors as seen in Figure 8) comprising using a multiprocessing computing system having a plurality of processors P to perform the steps (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) and for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency among the parallel processors (e.g. abstract and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a method comprising using a multiprocessing computing system having a plurality of processors P to perform the steps and for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency among the parallel processors as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claim 2, Abel et al. fail to disclose in Figures 1-14 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor. However, Jaber discloses in Figures 8-9 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor (e.g. col. 7 lines 2-30).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 3, it is a system claim having similar limitations of claim 1. Thus, claim 3 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 4, it is a system claim having similar limitations of claim 2. Thus, claim 4 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 5, Abel et al. disclose in Figures 1-14 a computer-readable storage medium whose contents cause a system having a plurality of processors to perform a

method of transforming a signal by computing with the plurality of processors a FFT or IFFT of the signal, the method comprising: computing a first plurality of stages of an N-point FFT/IFFT (e.g. first stage of Figure 4); and computing a second plurality of stages of the N-point FFT (e.g. next stage of Figure 4) without employing nested loops (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT).

Abel et al. fail to disclose in Figures 1-14 the distributing the plurality of butterfly operations in each stage of the second plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency. However, Jaber discloses in Figures 8-9 (e.g. by means of independent and distribute among processors as seen in Figure 8) the distributing system (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) the plurality of butterfly operations in each stage of the second plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency (e.g. abstract and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the distributing the plurality of butterfly operations in each stage of the second plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency as seen in Jaber's invention into Abel et al.'s invention because it would

enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claim 6, it has similar limitations cited in claim 2. Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 7, Abel et al. further disclose in Figures 1-14 the second plurality of butterfly operations have a radix-2 radix (e.g. component 800 in Figure 8 wherein the component 800 utilizes radix-2 to compute the butterfly computation of IFFT).

Re claim 11, Abel et al. fail to disclose in Figures 1-14 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location. However, Jaber discloses in Figures 8-9 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location (e.g. col. 15 lines 4-35).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 12, it is a system claim having similar limitations of claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, Abel et al. further disclose in Figures 1-14 computing a first and second stage of logzN stages of the N- point FFT/IFFT as a single radix-4 butterfly operation (e.g. component 900 in Figure 9).

Re claim 15, it is a system claim having similar limitations of claim 11. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 16, it is a computer-readable memory claim having similar limitations of claim 1. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a computer-readable memory claim having similar limitations of claim 2. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 18, it is a computer-readable memory claim having similar limitations of claim 11. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 27, Abel et al. disclose in Figures 1-14a method of transforming a digital signal (e.g. abstract and col. 1 lines 30-40), the method comprising: compute a first number of butterfly stages of an N-point Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT and either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively); and compute remaining butterfly stages of the N-point

FFT/IFFT wit a single iterative loop (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT).

Abel et al. fail to disclose in Figures 1-14 a multiprocessing computing system having a plurality P of processors and each processor (e.g. Figure 8) computes an equal number of butterfly operations and there is no data dependency between butterflies in a stage of an iteration of the loop. However, Jaber discloses in Figures 8-9 a multiprocessing computing system having a plurality P of processors and each processor computes an equal number of butterfly operations and there is no data dependency between butterflies in a stage of an iteration of the loop (e.g. abstract and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a multiprocessing computing system having a plurality P of processors and each processor computes an equal number of butterfly operations and there is no data dependency between butterflies in a stage of an iteration of the loop as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claims 28-29, Abel et al. fail to disclose in Figures 1-14 the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage and the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages. However, Jaber discloses in Figure 8 the

plurality of processors comprises two processors and the first number of butterfly stages consists of one stage (e.g. Figure 8 with only two processors A and B) and the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages (e.g. Figure 8 with only four processors as indicated by dot ….).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage and the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages as conceptually seen in Jaber's invention into Abel et al.'s invention because it would enable to reduce the computational burden in signal processing (e.g. col. 1 lines 44-52).

Re claim 31 it is a system claim having similar limitations of claim 27. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 27.

Re claim 32 it is a system claim having similar limitations of claim 28. Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 28.

Re claim 33 it is a system claim having similar limitations of claim 29. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 29.

Response to Amendment

8. The amendment filed 11/12/2009 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Re claims 1, 3, 5, 16, 27 and 31, the limitations "wherein each of the butterfly operations in each stage in the second set of stages has a single, un-nested computation loop" within these claims are not fully described in the original specification which introduce new matter into the disclosure of the invention.

Further, Figure 6 and its newly added description in pages 2-3 filed 06/21/2010 are considered new since they are not fully described in the original specification.

Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

9. Applicant's arguments filed 06/21/2010 have been fully considered but they are not persuasive.

a. The applicant argues in pages 11-15 that the newly added Figure 6 along with its newly added description would overcome the drawing objection.

The examiner respectfully submits that Figure 6 does not show the limitation "each stage in the second set of stages has a single, un-nested computation loop" and further the newly added paragraphs in pages 2-3 filed 06/21/2010 is

considered new since the context of the paragraph are not fully disclosed in the original specification.

b. The applicant argues in pages 16-17 that the original specification does not provides the support for the claims since it is known in the art as the difference between nested and un-nested loops in general.

The examiner respectfully submits that the specification MUST provide sufficient evidence or sufficient written description to enable the invention as required. Without the written enablement of the limitation, one would not know how to perform or obtain the limitation of "each of the butterfly operations in each stage in the second set of stages has a single, un-nested computation loop".

c. The applicant argues in pages 30-32 for all independent claims that Jaber fails to disclose the claimed invention, particularly the limitations of "distributing the plurality of butterfly operations in each stage....thereby eliminating data interdependency among the parallel processors" since N/2 coefficients are needed by all of the processors of Jaber all of the time and the entire set is needed by the combinational phase.

The examiner respectfully submits that the applicant has mis-understood the examiner's rejection and responses. Based on the claimed language, there requires a step of distributing butterfly operations in each stage for each processor wherein each processor operates equal number of butterfly operations, THEREBY eliminating data interdependency among the parallel processors. These

limitations are clearly seen in Jaber wherein combination phase is not part of the butterfly operations but rather the butterfly operation within the stage as seen in Figures. Figures 1 show that if each processor performs its own radix DFT with its own input coefficients and output coefficients, there is no data/coefficients dependency. Further, Figures 5 shows radix-R DIF module for performing butterfly operations that do not require data/coefficients from other parallel radix-R DIF module, thus there is no data/coefficients dependency. Therefore, the processors can operate in parallel as independently.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

August 23, 2010